IN THE CLAIMS

1. (Currently Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer, an etchstop layer applied to the first organic intermetal dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide;

forming a via opening in said stack;

depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially ~~filling~~ fills the via opening and substantially ~~covering~~ covers the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a line opening in the stack and the sacrificial inorganic dielectric, said line opening substantially aligned with said via opening;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

2. (Original) The method of Claim 1 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

3. (Original) The method of Claim 1 wherein said sacrificial inorganic dielectric is a methylsiloxane.

4. (Previously Presented) The method of Claim 1, wherein either the first or second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

5. (Previously Presented) The method of Claim 1 wherein said stack further comprises a diffusion barrier layer between said substrate and said first organic intermetal dielectric layer.

6. (Original) The method of Claim 5 wherein said diffusion barrier layer comprises silicon nitride.

Claims 7-12: Canceled.

13. (Currently Amended) The method of Claim 1 wherein depositing a stack comprises depositing a stack having a top surface on a substrate, wherein the stack comprises a diffusion barrier layer, an inorganic intermetal dielectric layer, an etchstop layer applied to the first inorganic intermetal dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide ~~said stack further comprises a diffusion barrier layer on said substrate, and inorganic intermetal dielectric layer between said diffusion barrier and said organic intermetal dielectric layer~~.

14. (Original) The method of Claim 13 wherein said diffusion barrier layer comprises silicon nitride.

15. (Original) The method of clam 13 wherein said inorganic intermetal dielectric layer comprises a material that comprises silicon oxide, fluorinated silicate glass, or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

16. Canceled.

17. (Original) The method of Claim 1 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

18. (Original) The method of Claim 1 wherein said conducting material comprises aluminum, copper, tungsten, or mixtures thereof.

19. (Original) The method of Claim 18 wherein said conducting material further comprises a conducting diffusion barrier material.

20. (Original) The method of Claim 1 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

21. (Original) The method of Claim 1 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.

22. (Currently Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer, an etchstop layer applied to the first organic intermetal dielectric layer, a second organic intermetal dielectric layer, and a hardmask layer, wherein the hardmask layer comprises a material comprising silicon oxynitride or silicon oxide;

forming a line opening in said stack;

depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially ~~filling~~ fills the line opening and substantially ~~covering~~ covers the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a via opening in the stack and the sacrificial inorganic dielectric;

selectively removing the sacrificial inorganic dielectric; and

filling the via opening and the line opening with conducting material.

23. (Original) The method of Claim 22 wherein said sacrificial inorganic dielectric comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, or mixtures thereof.

24. (Original) The method of Claim 22 wherein said sacrificial inorganic dielectric is a methylsiloxane.

25. (Previously Presented) The method of Claim 22, wherein wherein either the first or second organic intermetal comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated amorphous carbon, or mixtures thereof.

26. (Currently Amended) The method of Claim 22 wherein said stack further comprises a diffusion barrier layer between said substrate and said first organic intermetal dielectric layer.

27. (Original) The method of Claim 26 wherein said diffusion barrier layer comprises silicon nitride.

Claims 28-30: Canceled.

31. (Currently Amended) The method of claim [[29]] 22, wherein the etchstop layer comprises a material comprising silicon oxide.

32. (Currently Amended) The method of Claim [[29]] 22, wherein the second organic intermetal dielectric layer comprises an organic dielectric that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers, fluorinated

amorphous carbon, or mixtures thereof.

33. Canceled.

34. (Original) The method of Claim 22 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

35. (Original) The method of Claim 22 wherein said conducting material comprises aluminum, copper, tungsten, or mixtures thereof.

36. (Original) The method of Claim 35 wherein said conducting material further comprises a conducting diffusion barrier material.

37. (Original) The method of Claim 22 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

38. (Original) The method of Claim 22 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.